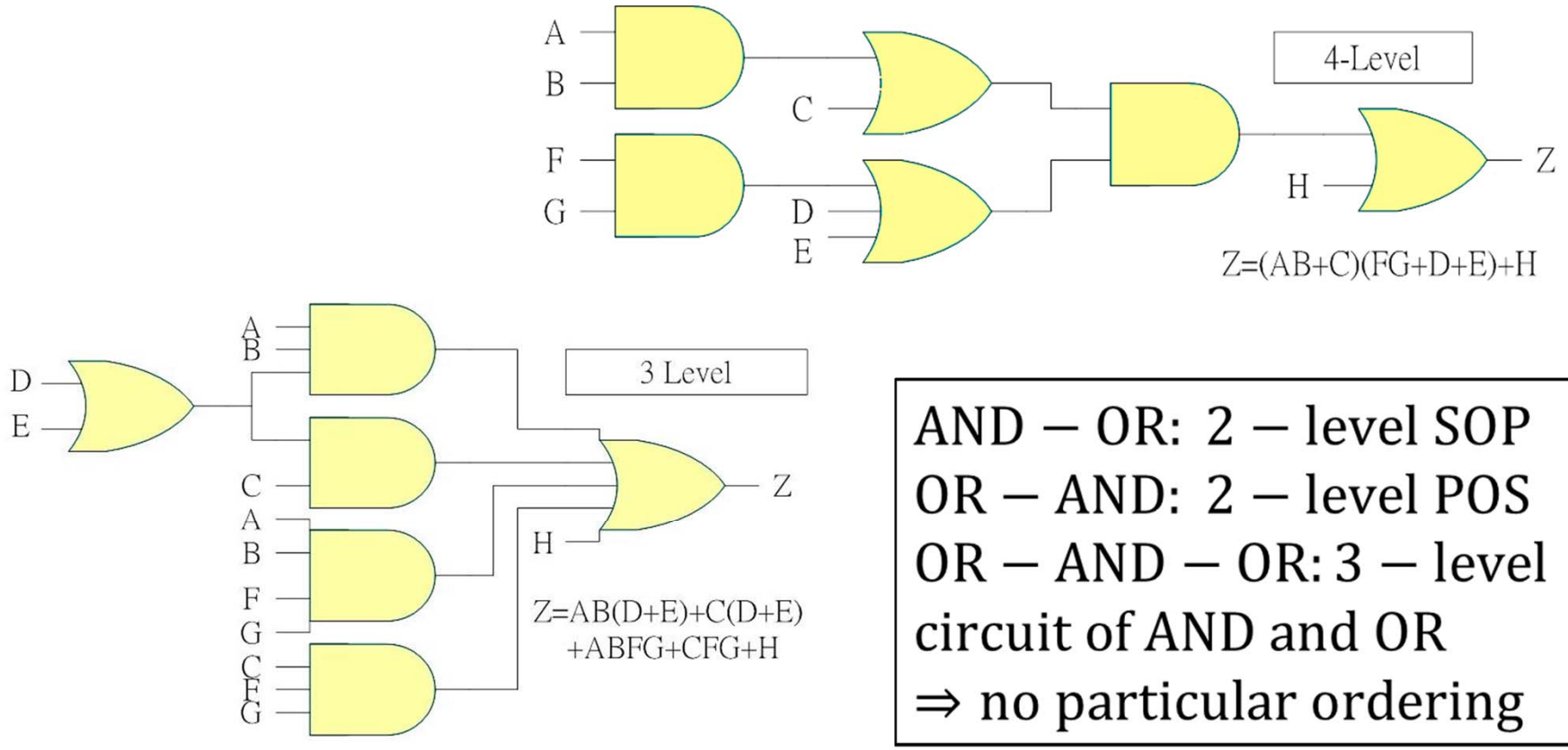
Unit 7

Multi-Level Gate Circuits / NAND and NOR Gates

Outline

- Multi-level gate circuits
- NAND and NOR gates
- 2-level NAND and NOR circuits
- Multi-level NAND and NOR circuits
- Multi-output circuit realization

Multi-Level Gate Circuits (1/2)

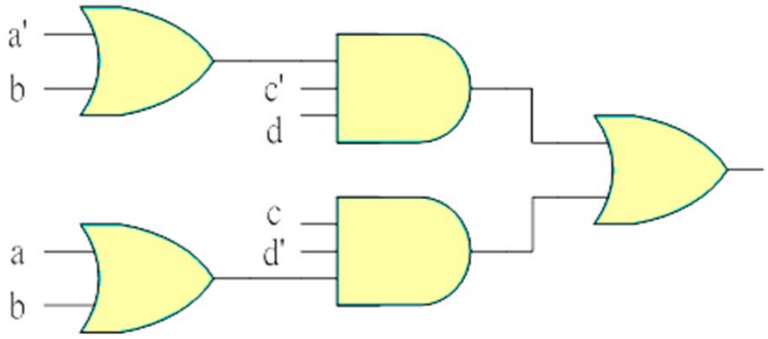


AND – OR: 2 – level SOP
OR – AND: 2 – level POS
OR – AND – OR: 3 – level circuit of AND and OR
⇒ no particular ordering

1. Gate input number & delay determine level
2. Factoring to accomplish different level

Multi-Level Gate Circuits (2/2)

$$f(a, b, c, d) = \sum m(1,5,6,10,13,14)$$



Using K-Map Method:

$$f = a'c'd + bc'd + bcd' + acd' \cdots\cdots (1)$$

2-level AND-OR gate network

$\Rightarrow$ 2 levels, 5 gates, 16 gate inputs

Factoring:

$$f = c'd(a' + b) + cd'(a + b) \cdots\cdots (2)$$

$\Rightarrow$ 3 levels, 5 gates, 12 gate inputs

or use POS:

$$f = (c+d)(a'+b+c)(c'+d')(a+b+c') \cdots (3)$$

$\Rightarrow$ 2 levels, 5 gates, 14 gate inputs

or $f = \left[c + d(a'+b)\right]\left[c' + d'(a+b)\right] \cdots (4)$

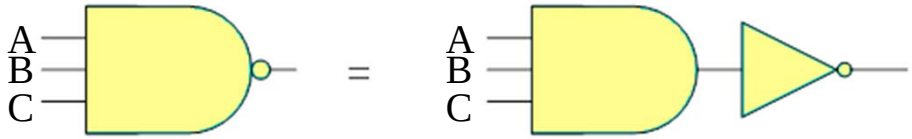
$\Rightarrow$ 4 levels, 7 gates, 14 gate inputs

or $f = \left[c + (a'd + bd)\right]\left[c' + (ad' + bd')\right] \cdots (5)$

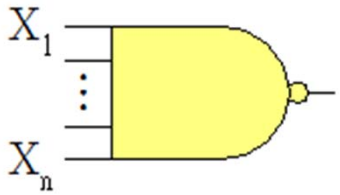
$\Rightarrow$ 3 levels, 7 gates, 16 gate inputs

NAND & NOR Gates (1/5)

NAND : F=(ABC)'=A'+B'+C'

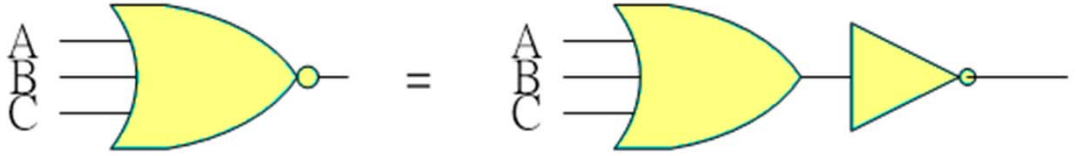


A	B	AB	$\overline{AB}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

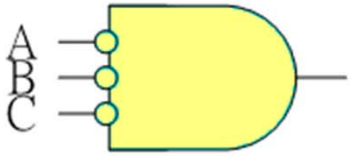


$$f = (x_1 \cdot x_2 \cdot \cdots \cdot x_n)' = x_1' + x_2' + \cdots + x_n'$$

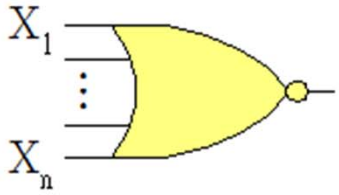
NOR :



F=(A+B+C)'=A'B'C' =



A	B	$A+B$	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0



$$f = (x_1 + x_2 + \cdots + x_n)' = x_1' \cdot x_2' \cdot \cdots \cdot x_n'$$

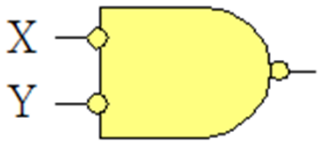
NAND & NOR Gates (2/5)

Functionally Complete Sets of Gates: A set of logic operations is Functionally Complete, if any Boolean function can be expressed in terms of this set of operations.

$\{\text{AND, OR, NOT}\}$

$\{\text{AND, NOT}\}$ $\because \text{OR} = X + Y = (X'Y')'$

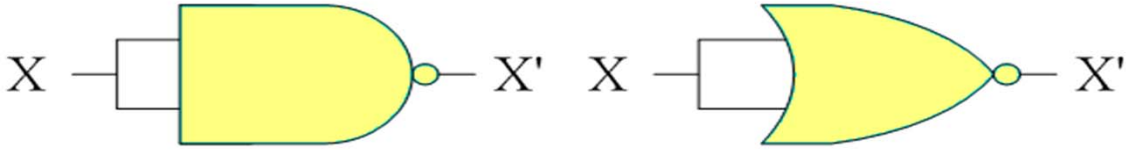
can be formed by AND, NOT



$\{\text{OR, NOT}\}$

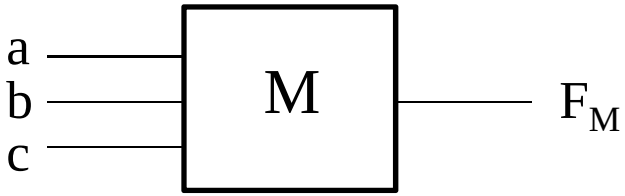
A functionally complete set of operations must contain NOT

NOT: Realized by NAND or NOR

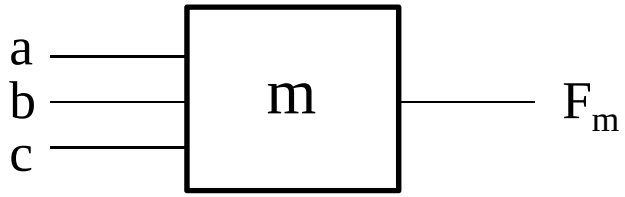


NAND & NOR Gates (3/5)

Majority Gate



Minority Gate

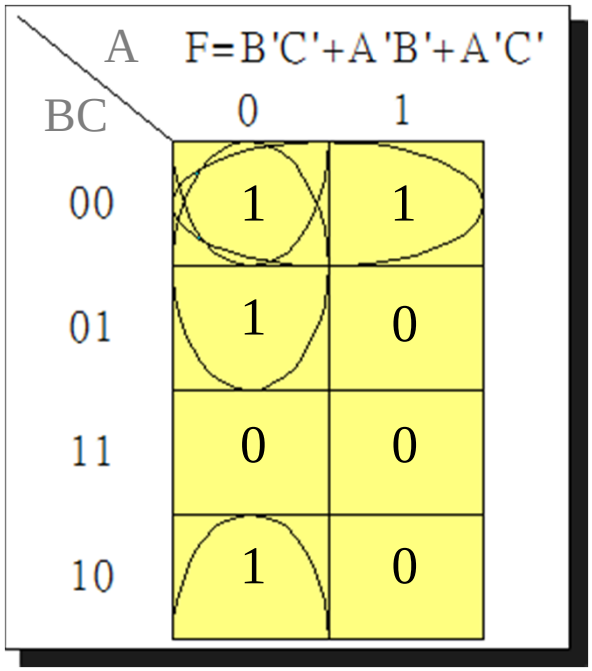


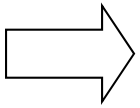
Odd number of inputs

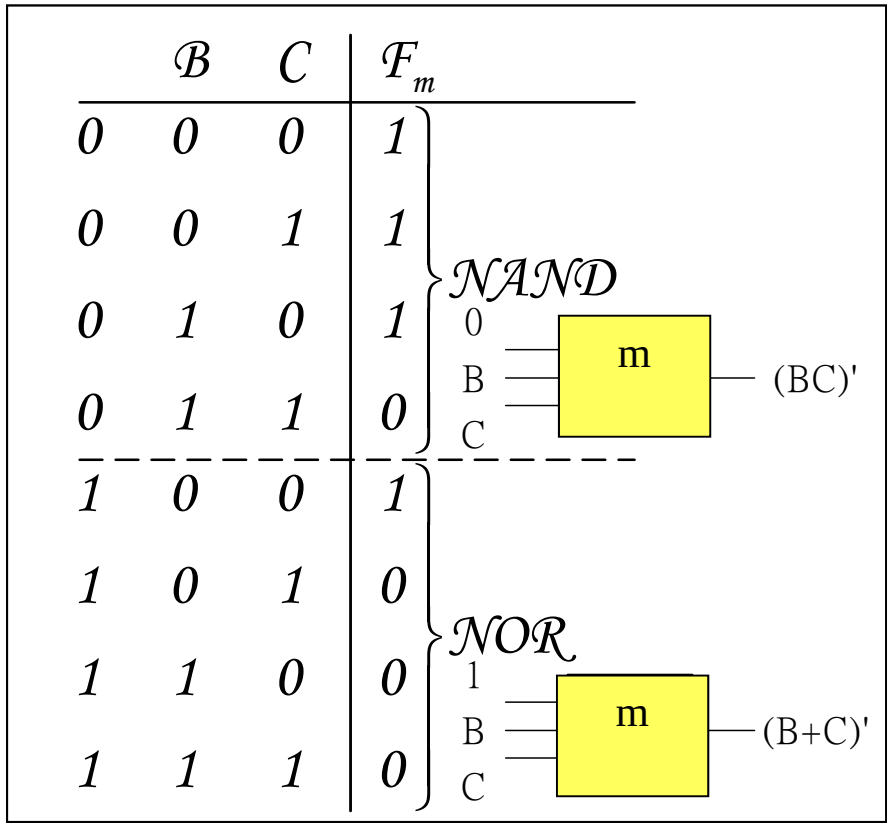
a	b	c	F_M	F_m
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

NAND & NOR Gates (4/5)

3-input minority gates can realize any switching function

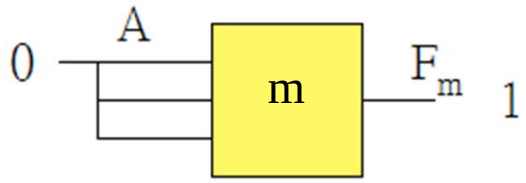




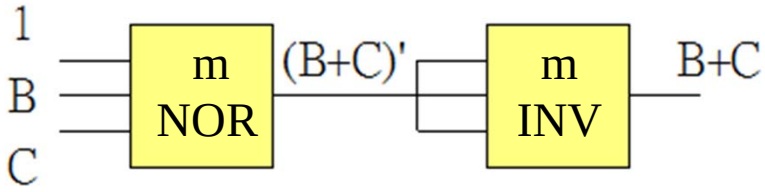


NAND & NOR Gates (5/5)

1. Inverter : Let C=B=A

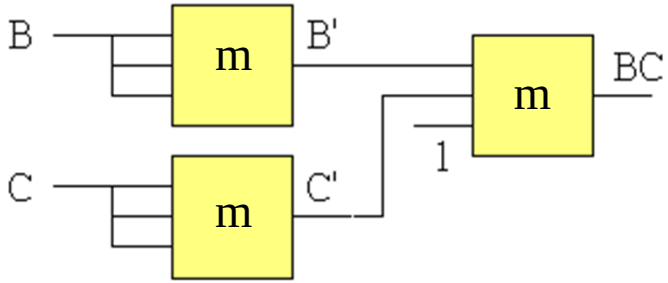


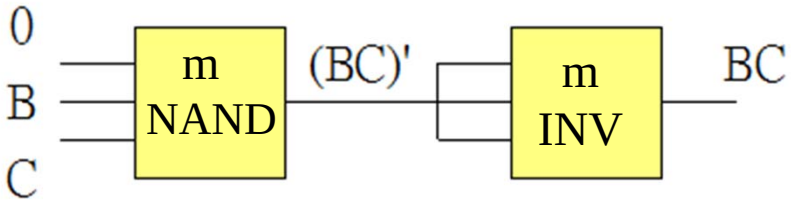
3. OR : B+C = 〔(B+C)'〕'



2. AND : Let A=1 then Fm =B'C'

Must invert B & C in advance

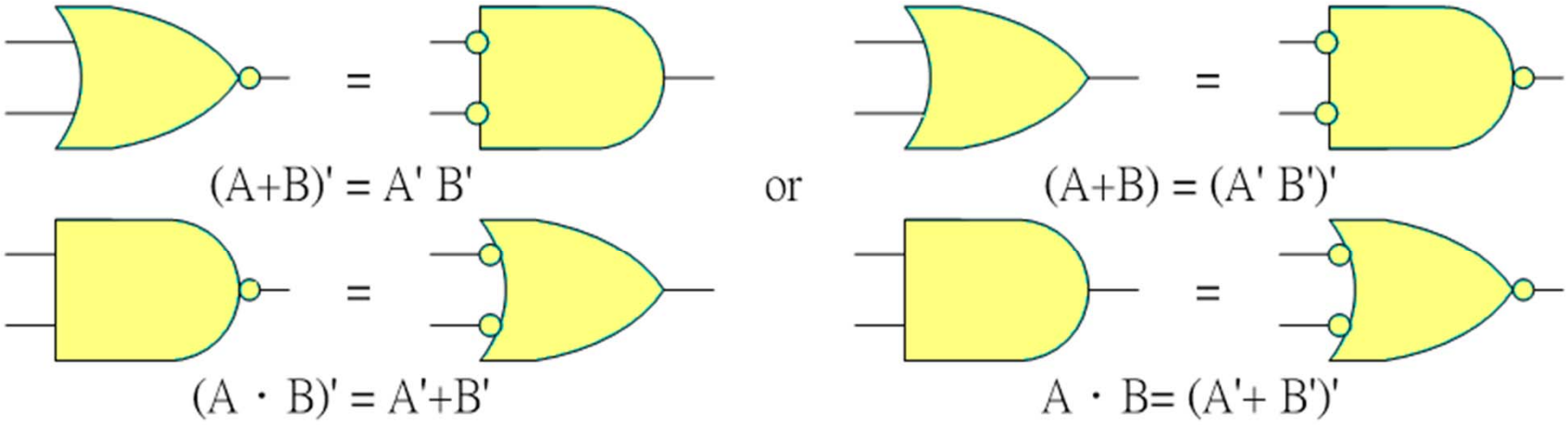




2-level NAND & NOR Circuits (1/3)

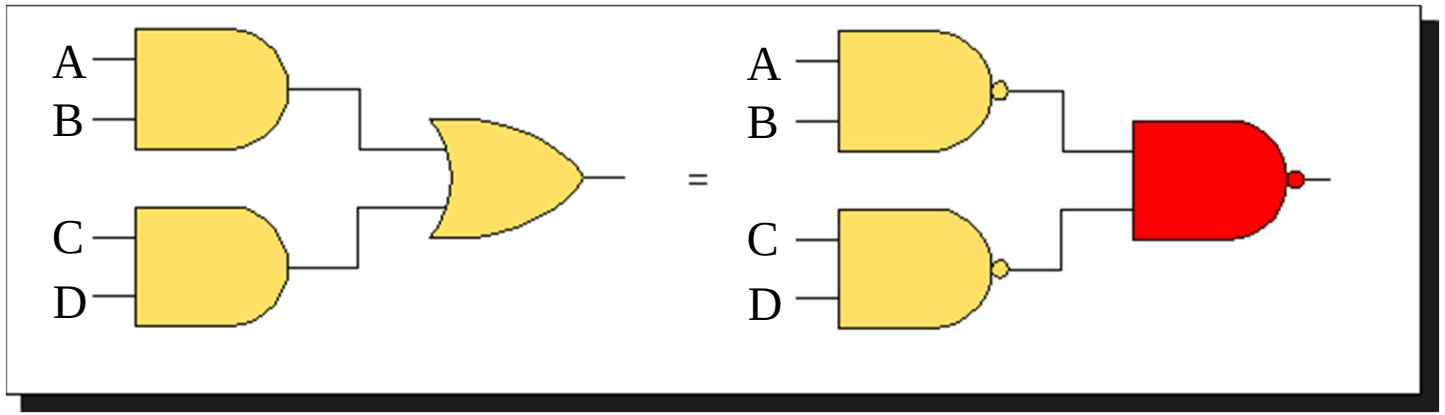
NAND & NOR : Readily available in IC form

DeMorgon's Law

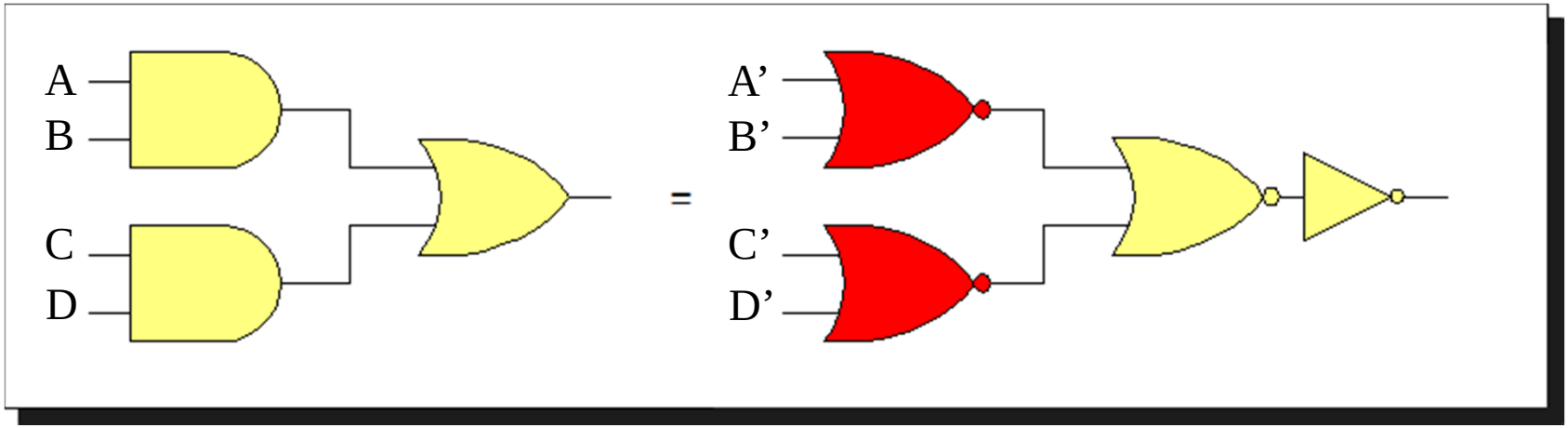


2-level NAND & NOR Circuits (2/3)

Ex1 : AND / OR ⇒ NAND/NAND

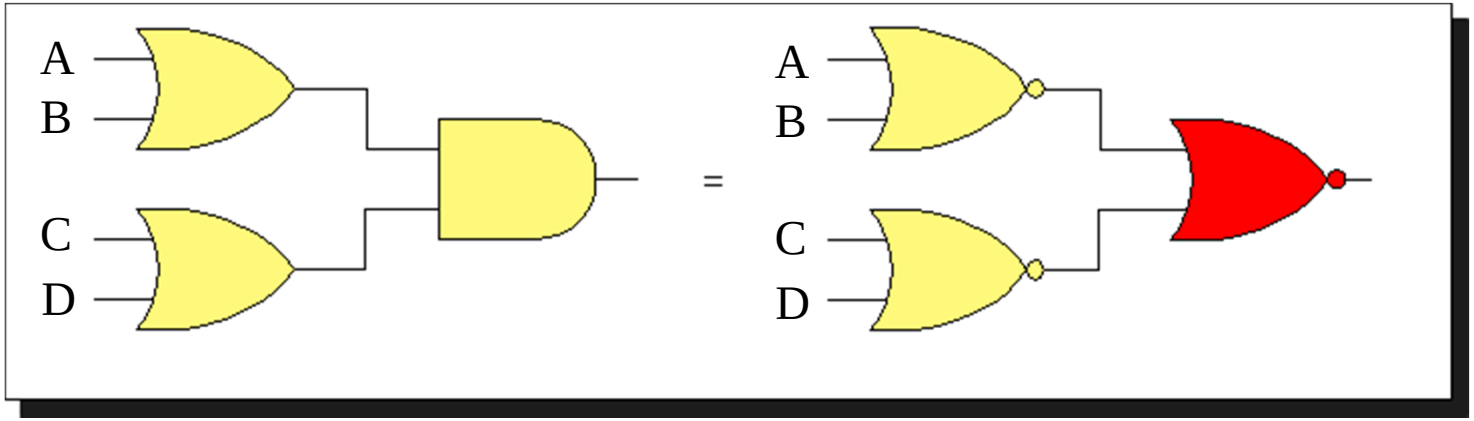


Ex2 : AND / OR ⇒ NOR/NOR

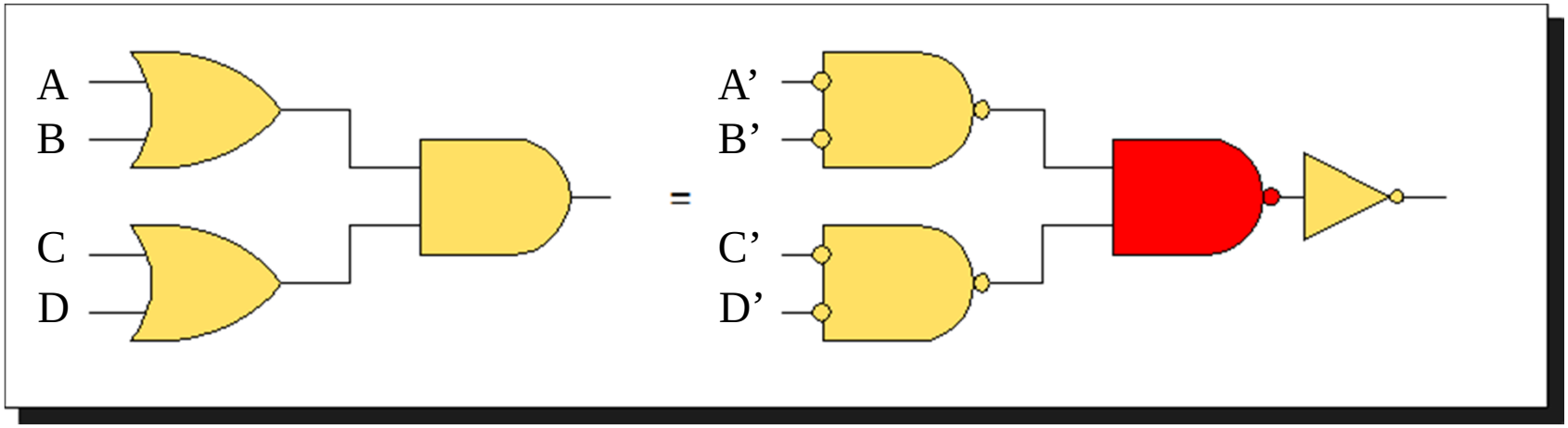


2-level NAND & NOR Circuits (3/3)

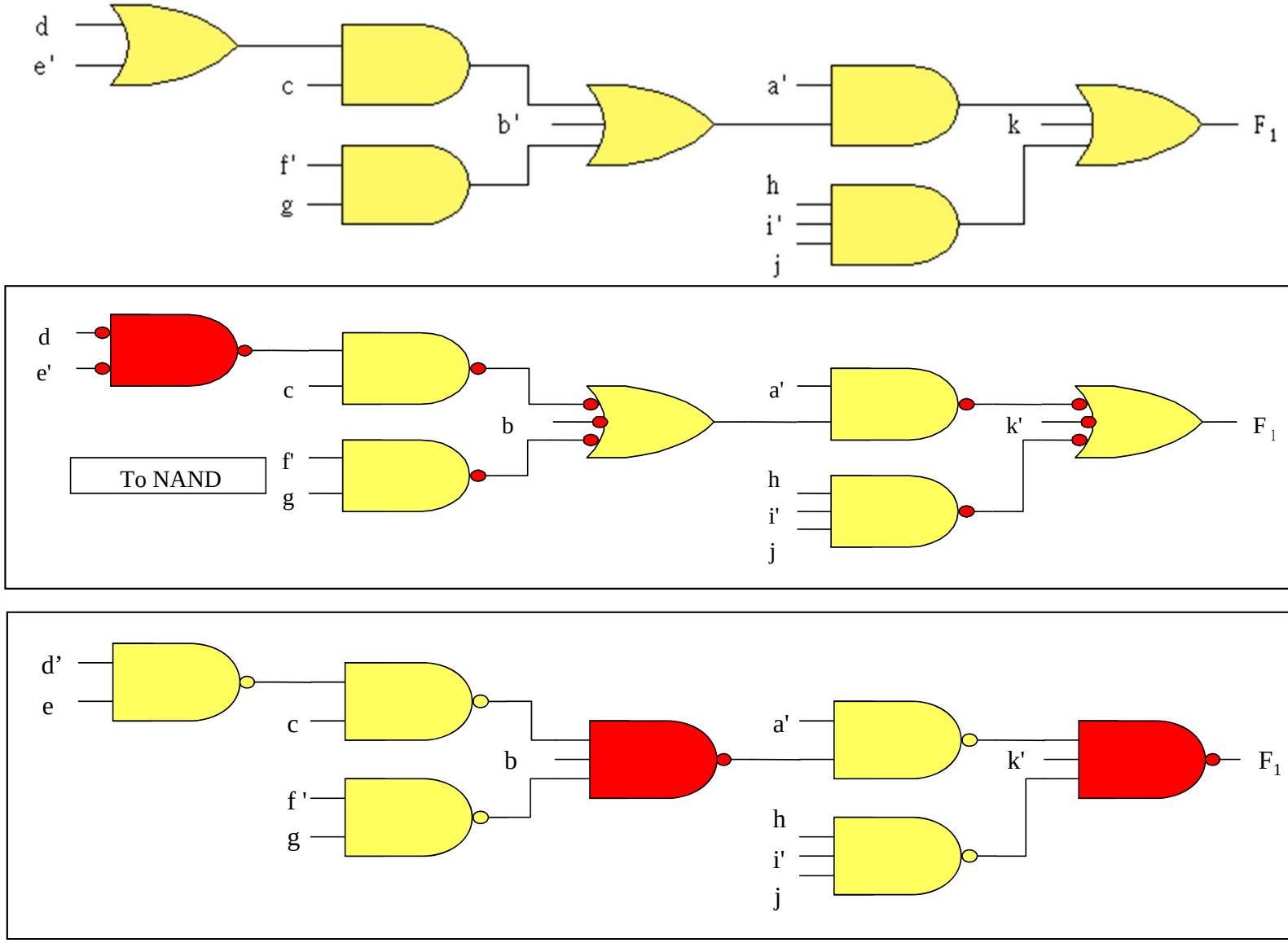
Ex1: *OR* / *AND* $\Rightarrow$ NOR/NOR



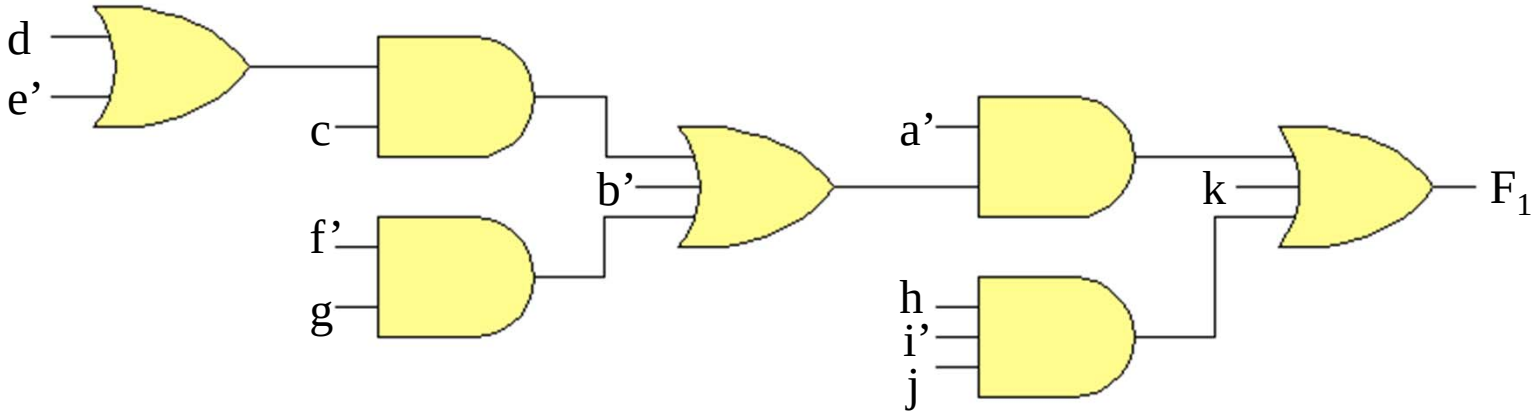
Ex2 : OR / AND $\Rightarrow$ *NAND/NAND*

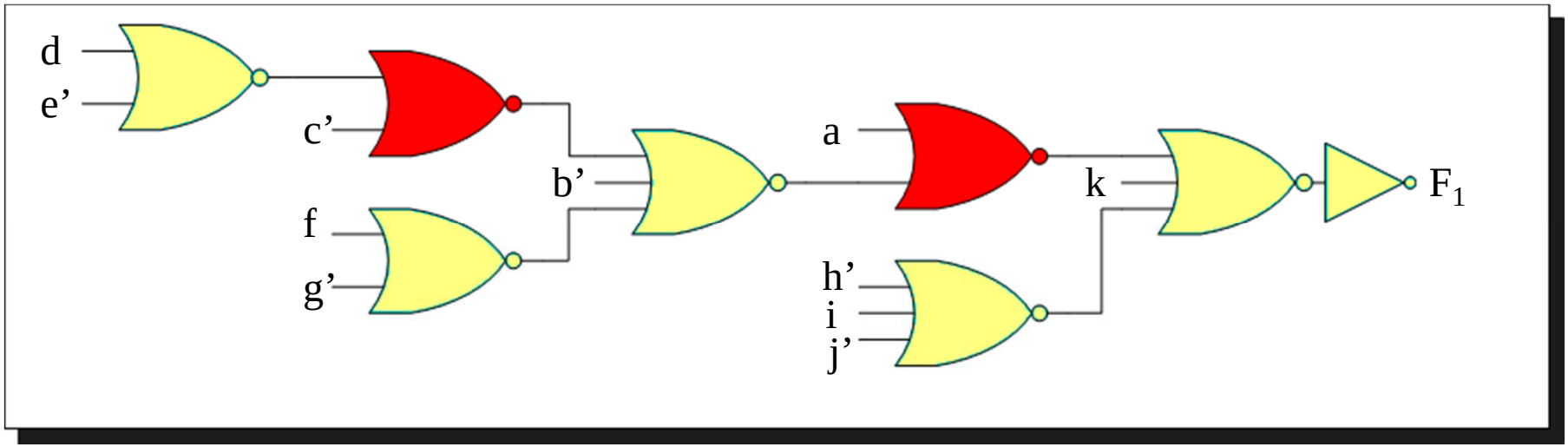


Multi-level NAND & NOR Circuits (1/2)



Multi-level NAND & NOR Circuits (2/2)





Multi-output Circuit Realization (1/11)

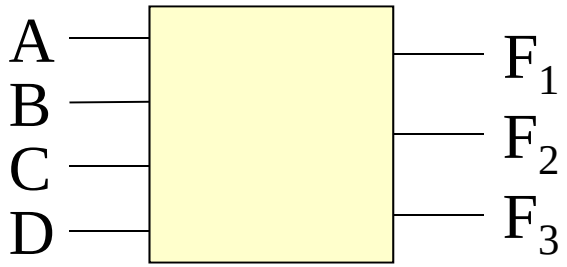
$$Ex: \quad F_1(A,B,C,D) = \sum m(11,12,13,14,15)$$
$$F_2(A,B,C,D) = \sum m(3,7,11,12,13,15)$$
$$F_3(A,B,C,D) = \sum m(3,7,12,13,14,15)$$

From K-Map

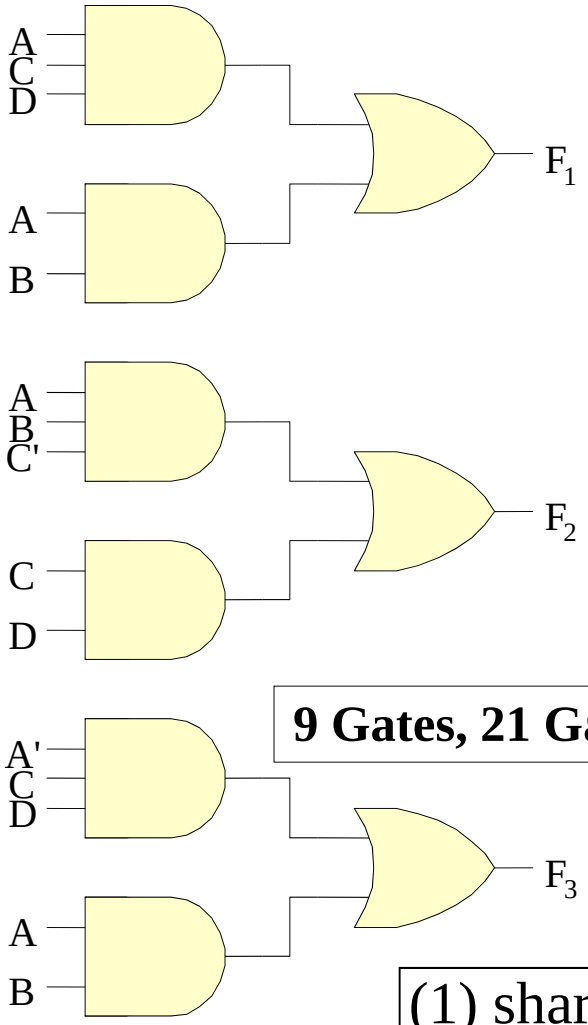
$F_1 = AB + ACD$

$F_2 = ABC' + CD$

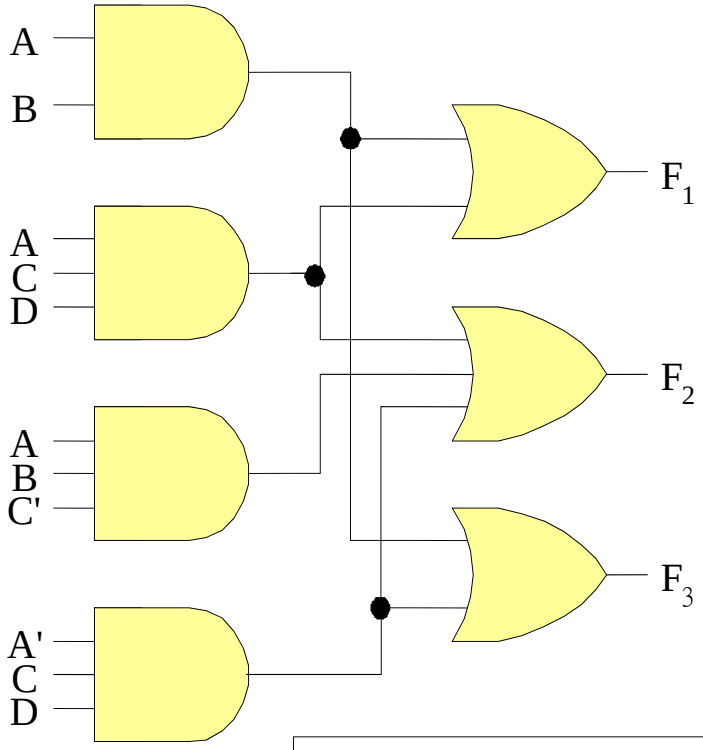
$F_3 = A'CD + AB$



Multi-output Circuit Realization (2/11)



9 Gates, 21 Gate inputs



7 Gates, 18 Gate inputs

(1) share AB

(2) A'CD + ACD = CD, CD covers A'CD and ACD

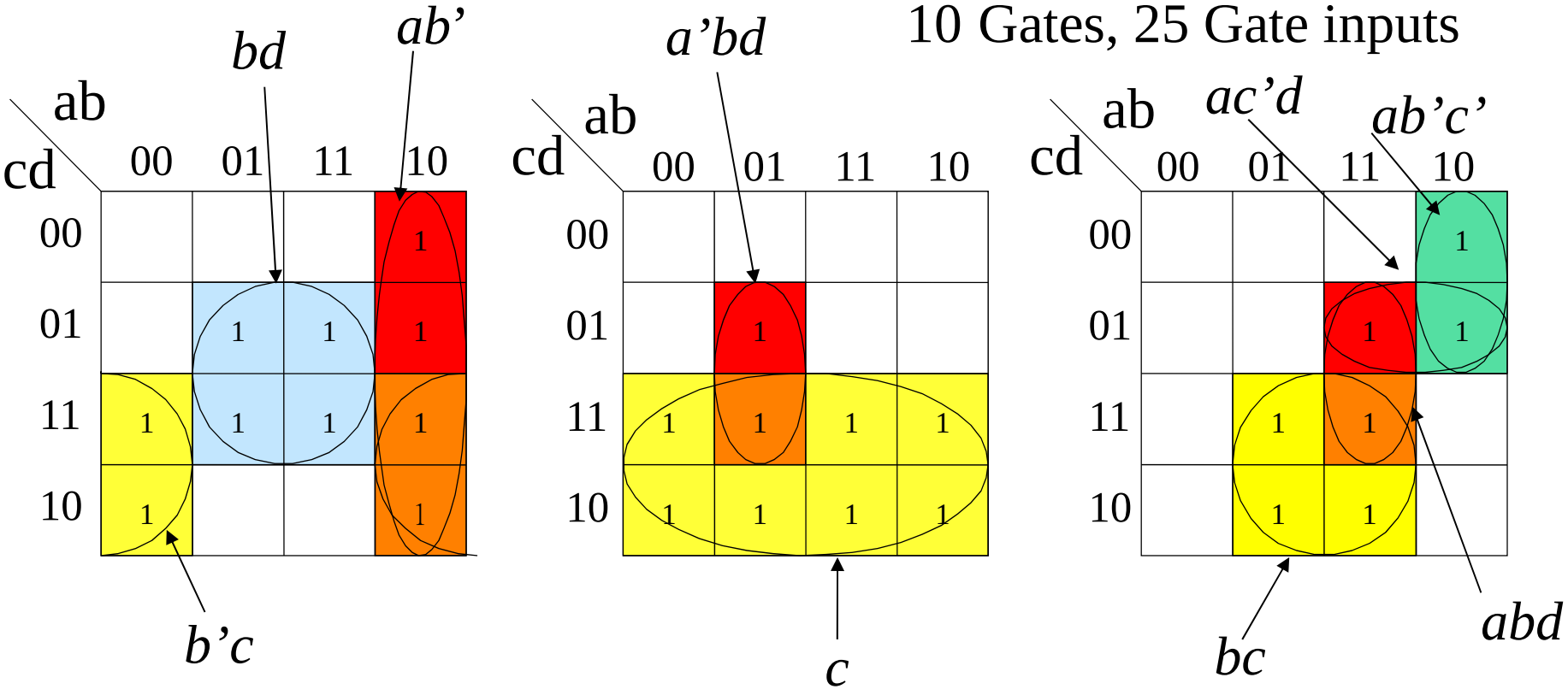
Multi-output Circuit Realization (3/11)

$$f_1 = \sum m(2, 3, 5, 7, 8, 9, 10, 11, 13, 15) \qquad f_1 = {}_1bd + {}_2b'c + {}_3ab'$$

$$f_2 = \sum m(2, 3, 5, 6, 7, 10, 11, 14, 15) \qquad f_2 = {}_4a'bd + c$$

$$f_3 = \sum m(6, 7, 8, 9, 13, 14, 15) \qquad f_3 = {}_5bc + {}_6ab'c' + {}_7\begin{cases} ac'd \\ abd \end{cases}$$

10 Gates, 25 Gate inputs



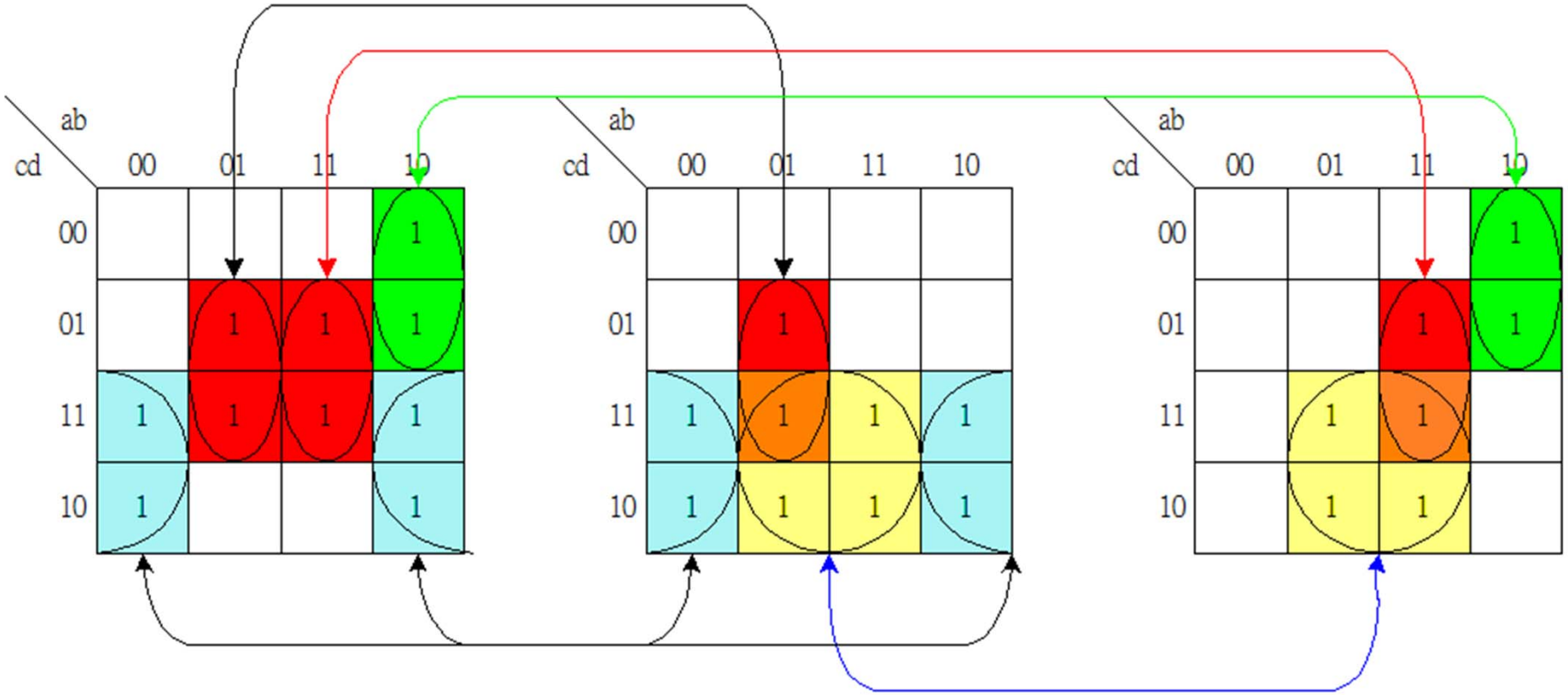
Multi-output Circuit Realization (4/11)

$$f_1 = {}_1a'bd + {}_2abd + {}_3ab'c' + {}_4b'c$$

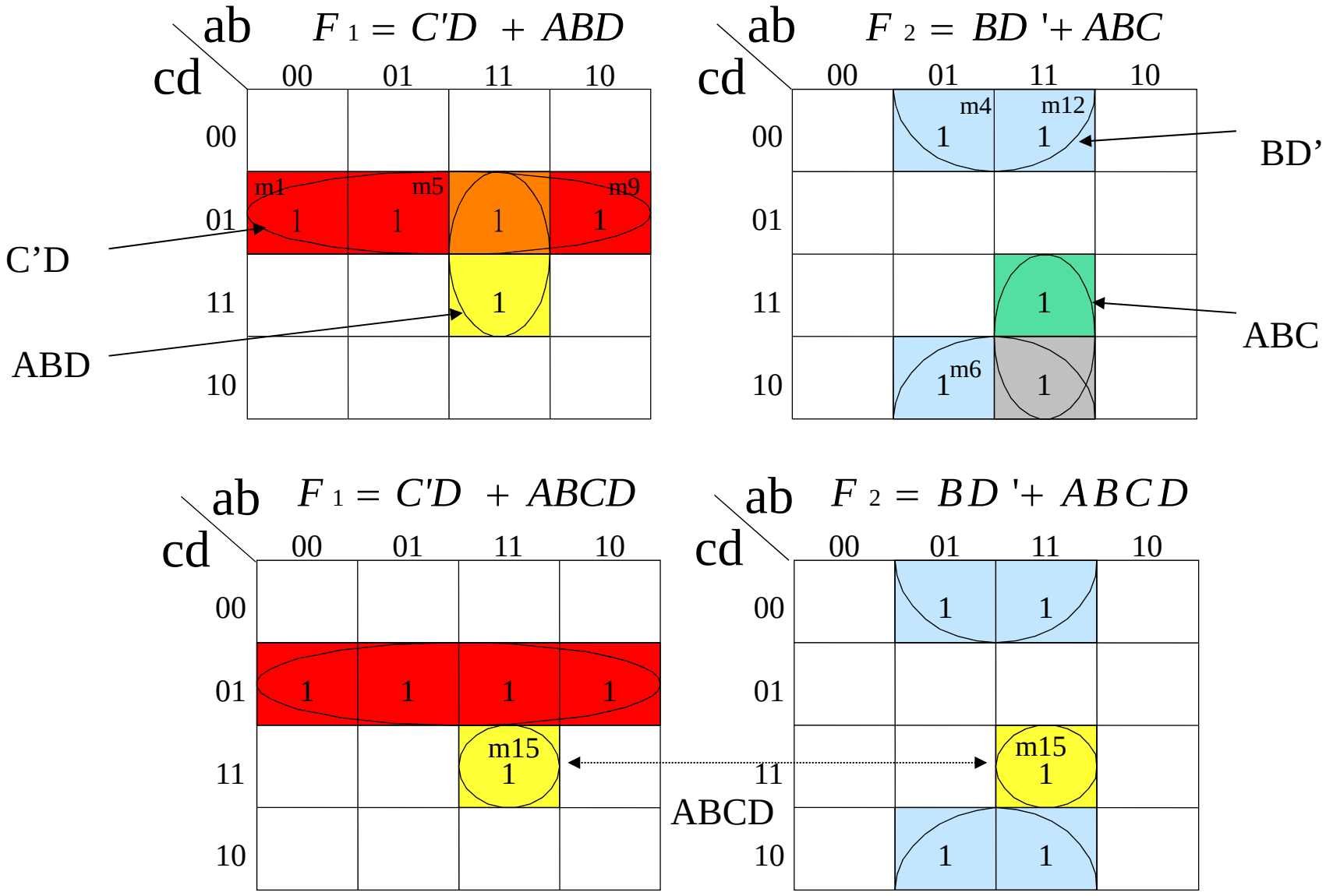
$$f_2 = {}_1a'bd + {}_4b'c + {}_5bc$$

$$f_3 = {}_3ab'c' + {}_2abd + {}_5bc$$

8 Gates, 23 Gate inputs



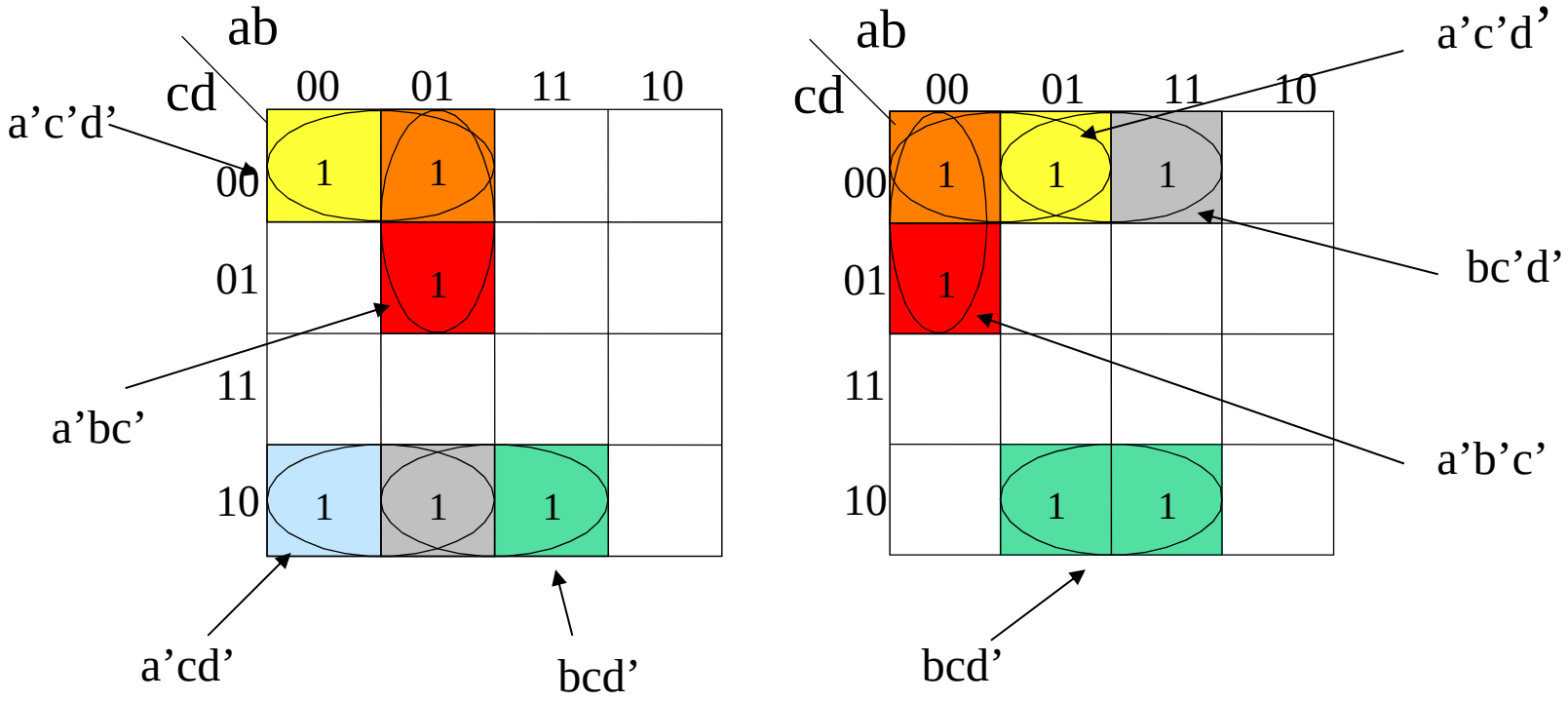
Multi-output Circuit Realization (5/11)



Multi-output Circuit Realization (6/11)

$F_1 = a'c'd' + a'bc' + a'cd' + bcd'$

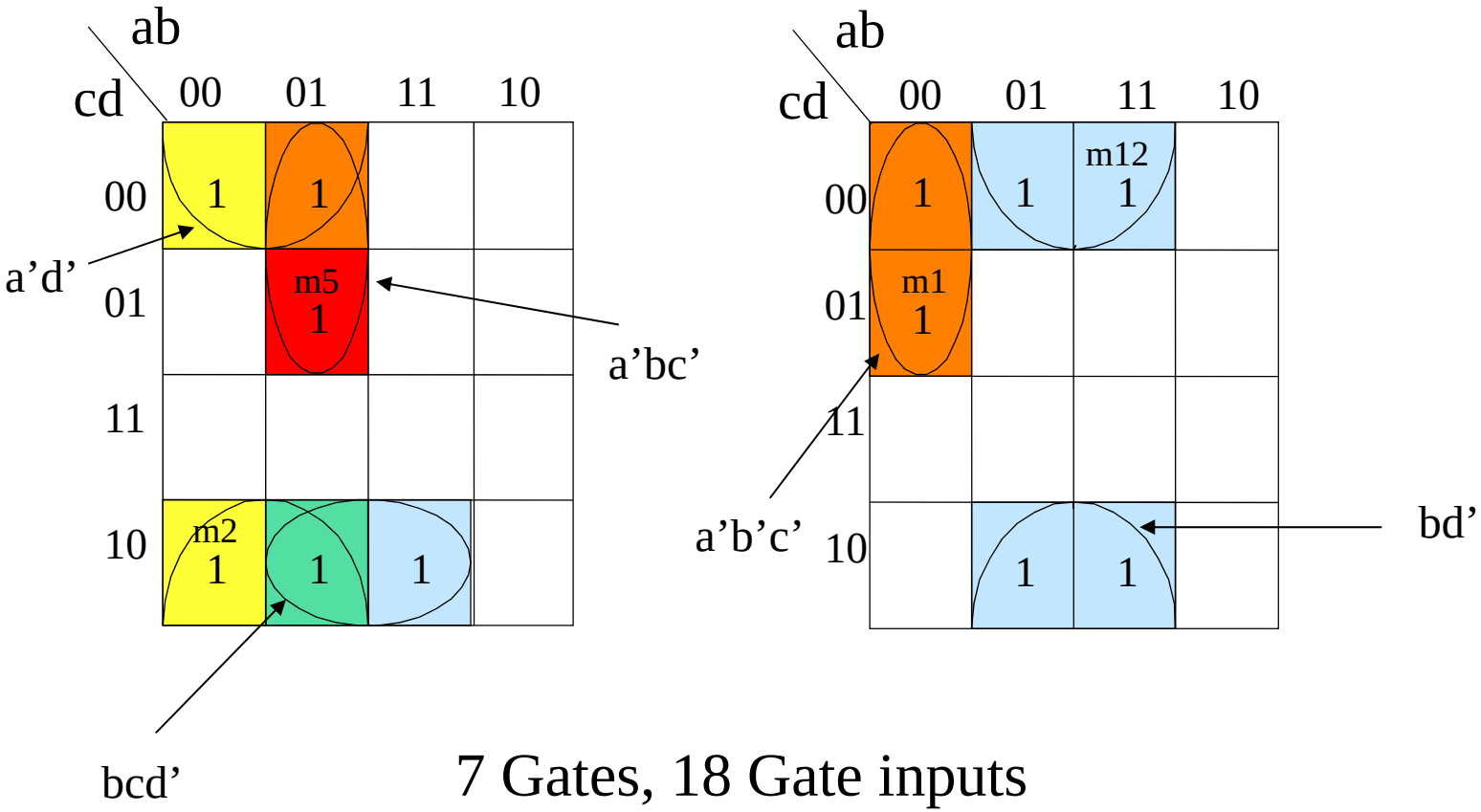
$F_2 = a'c'd' + bc'd' + a'b'c' + bcd'$



8 Gates, 26 Gate inputs

Multi-output Circuit Realization (7/11)

$$F_1 = a'd' + a'bc' + bcd' \qquad F_2 = a'b'c' + bd'$$



7 Gates, 18 Gate inputs

Multi-output Circuit Realization (8/11)

Determine *essential prime implicants* for multiple output function

On (5/11), c'd (m_1, m_5, m_9), bd' (m_4, m_6, m_{12}) are essential,

abd, abc are not essential.

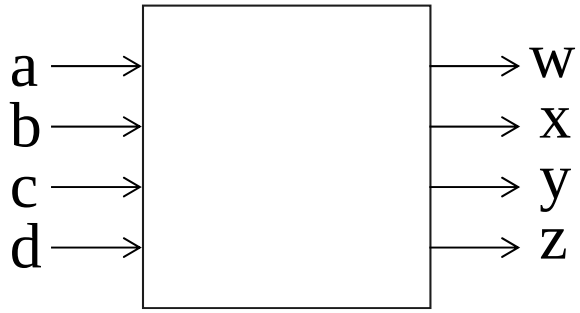
$\because m_{15}$ is in abd of F_1, and in abc of F_2.

On (7/11), a'd' (m_2), a'bc' (m_5), a'b'c' (m_1), bd' (m_{12}) are essential.

Generally, do not split essential terms for sharing

Multi-output Circuit Realization (9/11)

8-4-2-1 BCD to Excess-3 Code



$$w = a + bc + bd$$

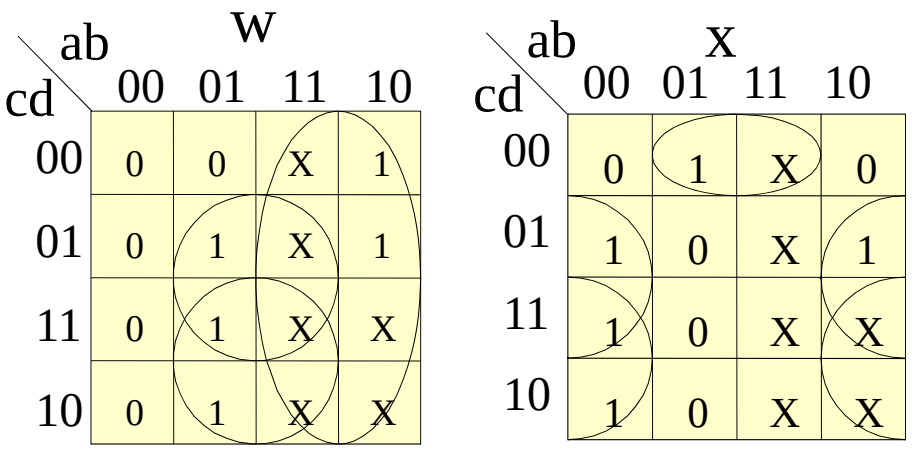
$$x = bc'\,d' + b'\,d + b'\,c$$

$$y = c'\,d' + cd$$

$$z = d'$$

a	b	c	d	w	x	y	z	
0	0	0	0	0	0	1	1	0
0	0	0	1	0	1	0	0	1
0	0	1	0	0	1	0	1	2
0	0	1	1	0	1	1	0	3
0	1	0	0	0	1	1	1	4
0	1	0	1	1	0	0	0	5
0	1	1	0	1	0	0	1	6
0	1	1	1	1	0	1	0	7
1	0	0	0	1	0	1	1	8
1	0	0	1	1	1	0	0	9
1	0	1	0	X	X	X	X	
1	0	1	1	X	X	X	X	
1	1	0	0	X	X	X	X	
1	1	0	1	X	X	X	X	
1	1	1	0	X	X	X	X	
1	1	1	1	X	X	X	X	

Multi-output Circuit Realization (10/11)



$$w = a + bc + bd$$

$$x = bc'd' + b'd + b'c$$

$$y = c'd' + cd$$

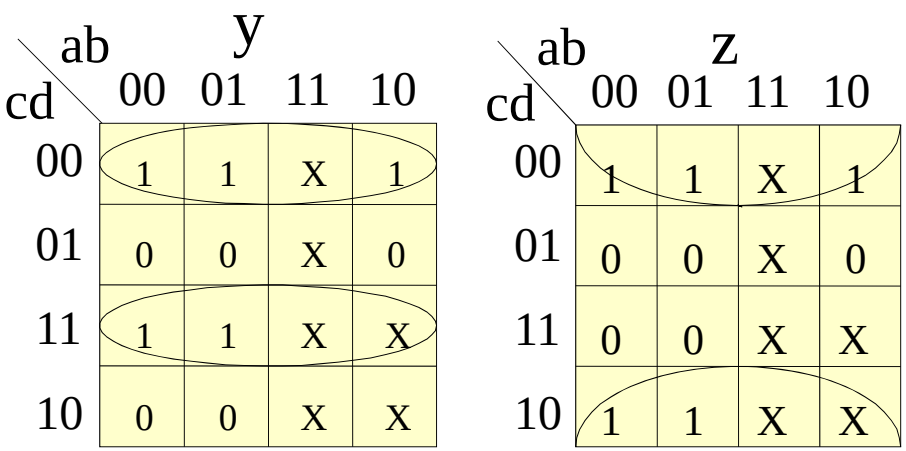
$$z = d'$$

3-Level Network

9 Gates

2-Level Network

10 Gates



$$w = a + b(c + d)$$

$$x = bc'd' + b'(c + d)$$

$$y = c'd' + cd$$

$$z = d'$$

Multi-output Circuit Realization (11/11)